LASER CHIP SEPARATION METHOD FOR GaAs MMIC WAFERS

by

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ABSTRACT

A chip separation process using a Nd-YAG laser with the wafer mounted on stretchable tape for machine sort and load has been developed for the GaAs MMIC wafers. This method is especially suitable for prototype masks with multiple chip design. One of the major advantages of this technique is that the laser can be programmed to cut any pattern desired such that the different circuits need not be laid out in a straight grid pattern as required for sawing. One hundred percent (100%) chip separation yield with no chipping or cracking has been demonstrated. The complete laser chip separation process will be described.

INTRODUCTION

In order to lower the GaAs IC development cost and to improve the prototype efficiency, multiple designs mask sets are quite often used. However, since the chip sizes and shapes for the various MMIC applications are significantly different (Fig. 1), it is impossible to layout chips in a straight grid pattern so that sawing could be used to separate circuits without sacrificing some of the chips. Use of a ND-YAG laser which can be programmed to cut any pattern eliminates this layout constraint. The idea is straight forward. However, to be able to implement it such that this can be done with the wafer mounted on stretchable tape so that automatic sort-and-load can be used to minimize chip handling problems and still have the separated chips looking as good and performing as well as they were before the process is a real challenge. This paper will describe such a laser chip separation process that has been successfully demonstrated with a 100% separation yield on a significant number of RF and MMIC wafers.

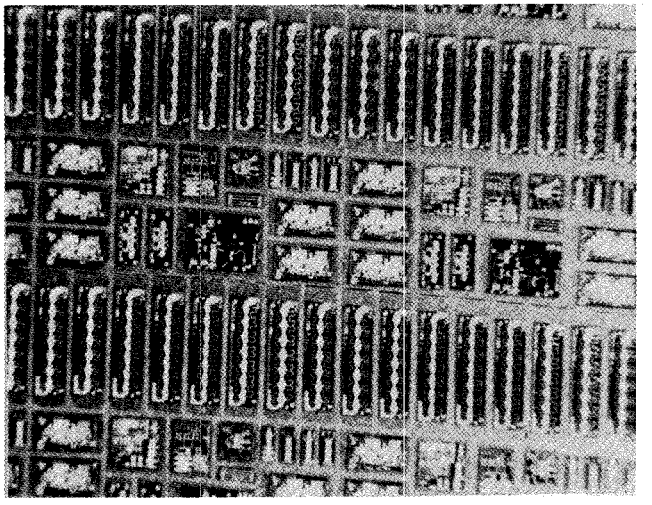

Fig. 1
Different MMICs from a multidesigner Mask Set. Wafer has been laser cut and stretched.

PROCESS SEQUENCE

The laser chip separation process sequence after the scratch protection layer has been completed is shown in Fig. 2.

- Scratch Protection Layer
- Front Scribe Alley Etch
- Backside Process
  Backlap
  Backside metal
  or
  Backlap
  Backside via holes
  Backside alley Au etch
- Wafer test
- Mount wafer on tape and frame
- Spin on protective coating
- Laser cut
- Remove protective coating
- Stretch and frame
- Sort and load

Fig. 2 Process Sequence for Laser Chip Separation

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As indicated in the process sequence, laser separation is compatible with backside vias. No noticable change in circuit performance was observed on circuit that has been through laser chip separation process. The heating effect does seem to be very localized (within a few micron of the cut), significantly away from the actual circuit area. (1)

PROCESS DESCRIPTIONS

(1) Front Scribe Alley Etch-

Since the Nd-YAG laser utilized does not have high enough power to completely vaporize the GaAs material, GaAs slag is formed around the circuit as the laser cuts through the GaAs crystal. This slag is about 10-15 um in height which causes problems in the subsequent chip handling and wire bonding operations. In order to minimize the adverse effect of this slag, a GaAs trough about 20-24 um deep is isotropically etched into the frontside scribe alley, (Fig. 3a and 3b), using photoresist as an etch mask. The trough keeps the slag formation below the surface of the circuit, (Fig. 4). As a result, the slag will not affect chip handling and bonding.

(2) Backside Process-

After the front scribe alley etch, the wafer is backlapped to a final wafer thickness of 4 ± 0.2 mils. For a wafer without backside via holes, a thin (4000 A) backside metal is deposited on the backside for chip die-attach purpose. Since the laser used can cut through the GaAs and this thin metal film on the backside, no additional process is required to remove this metal film from the backside scribe alley. For wafers with backside via holes, four to ten micron thick plated Au is used to connect these via holes. In order to obtain consistent chip separation, this thick Au film is etched out of the backside scribe alley.

(3) Wafer Test-

At this stage, the dismounted wafer is tested both for its DC and RF characteristics. Wafer passing the yield criteria will then be ready for laser chip separation.

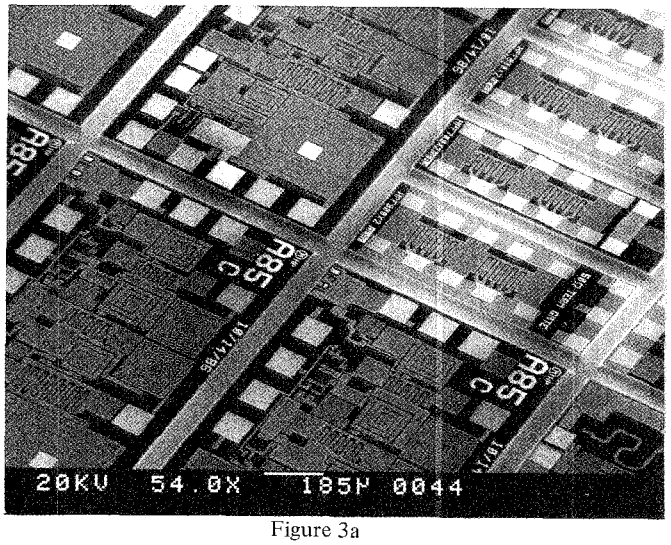

Figure 3a
23um deep isotropically etched trough in the frontside scribe alley. Overiew (a), close up (b).

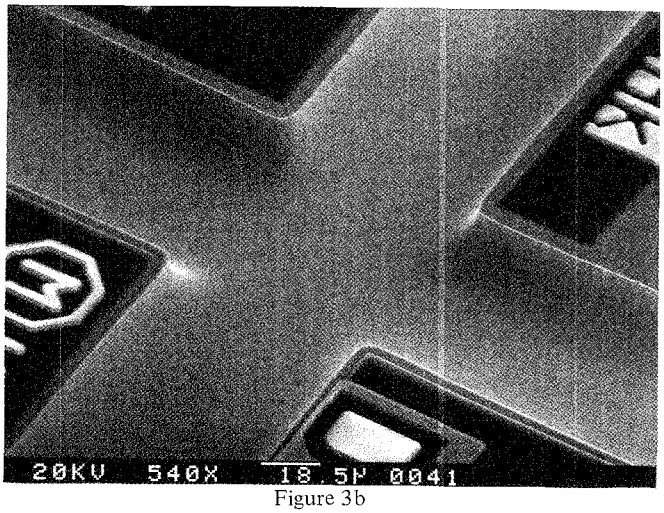

Figure 3b

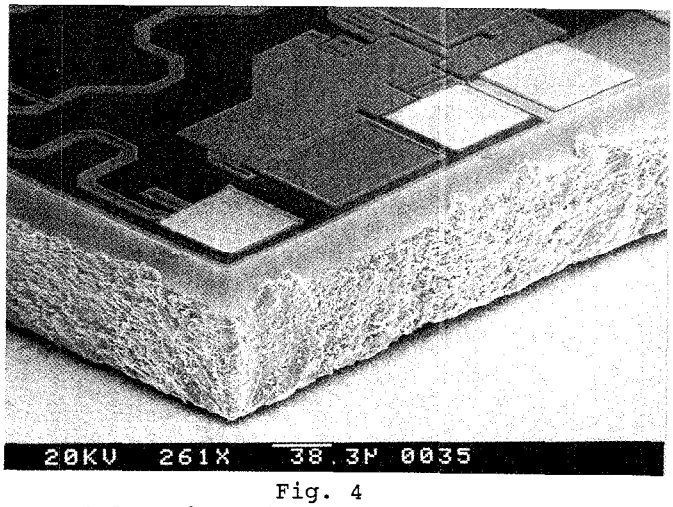

Fig. 4
GaAs slag forms below the surface of the circuit.

(4) Wafer Mounting-

The wafer is mounted face up onto a standard adhesive tape typically used for wafer sawing and the tape is stretched onto a 6"x 6" metal frame, as shown in Fig. 5. A special chuck was designed to minimize the risk of cracking the wafer during this mounting operation. The quality of this tape needs to be monitored from lot to lot in order to ensure consistent process results. Some of the critical parameters which are monitored are: the tackiness of the adhesive, the elasticity of the tape, the amount of tape damage caused by the laser beam due to imperfections in the tape and the ability to attach the stretched tape to metal frame for sort-to-load if glue is used.

(5) Protective Coating-

As the laser cuts through the GaAs wafer it will generate debris of GaAs along its way. The amount of debris depends greatly on the laser parameters used as well as how well the laser beam is aligned. In order to allow subsequent removal of the debris from the wafer, a thick layer of photoresist (~9um) is spun on the wafer and the tape, Fig. 5. The photoresist is then air dried for about 12 hours before laser cutting for optimal separation.

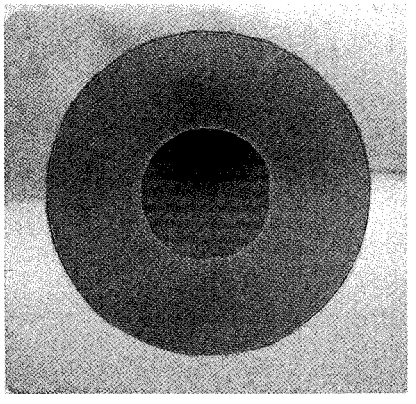

Fig. 5
Wafer mounted on tape and frame with PR protective coating spun on.

(6) Laser Cutting-

Using our Nd-YAG laser system, a matrix of experiments was carried out to identify the optimal laser parameters for cutting GaAs wafers. Some of the critical parameters used are listed in Table I.

Type of Laser	Nd-YAG Laser
Wavelength	1064 nm
Average Power	0.85W@4KHz
Power Density	120 KW/cm^2
Spot Size	0.75-1 mil
Laser Mode	TEM00
Cut Rate	8 mm/sec
Q Switched Rep Rate	4 KHz
Focus	1 mil below GaAs surface
Moving Beam Computer Controlled System	
In-House Fabricated Station	
In-House Developed Software	

TABLE I

Even with these optimal laser parameters, the laser will produce photoresist residue when the laser beam first hits the fresh GaAs surface. In order to avoid this, a cutting sequence with the following criteria has to be used for each reticle pattern: (1) Start the first laser cut on the tape and then cut into the wafer; (2) Within the reticle cutting, always start a new cut on a previously cut alley. A two-pass approach is also used for each reticle to ensure a 100% chip separation.

(7) Protective Coating Removal-

Since this adhesive tape is made up of Poly Vinyl Chloride, it is extremely sensitive to any solvent-based positive photoresist stripper. Therefore, alkaline based positive photoresist stripper is used to strip the protective photoresist coating. Fig. 6a and 6b show the same location on the wafer before and after the protective coating is removed. As can be seen, the circuits after the removal look very clean. Fig. 7 shows a close up view of the laser cut before the wafer is expanded. The kerf loss is about 27 microns wide.

(8) Stretch and Frame-

At this point, the tape is carefully peeled off the frame and then stretched on the wafer expanding equipment. Finally, another metal frame is then glued onto the stretched tape for the sort and load machine. Fig. 8 shows one of the laser scribed wafers that has some of the circuit removed using this technique.

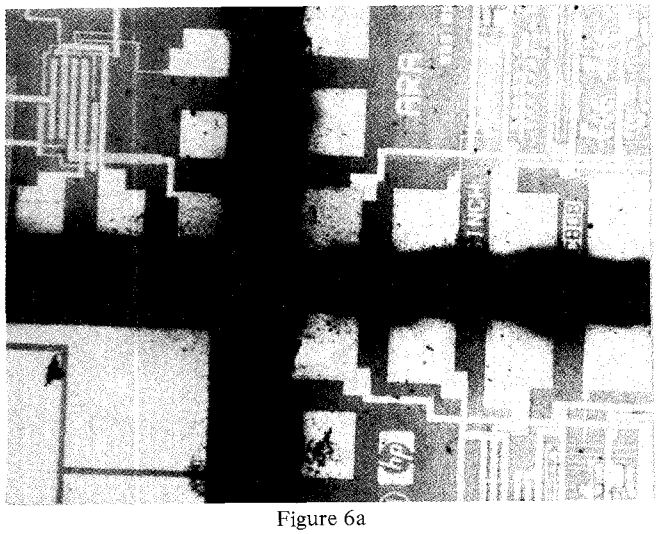

Figure 6a

At the same location on the wafer. Before (a) and after (b) protective coating removal.

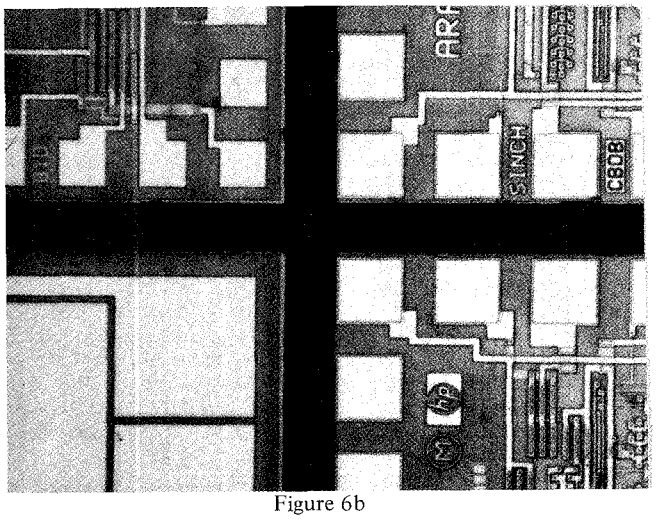

Figure 6b

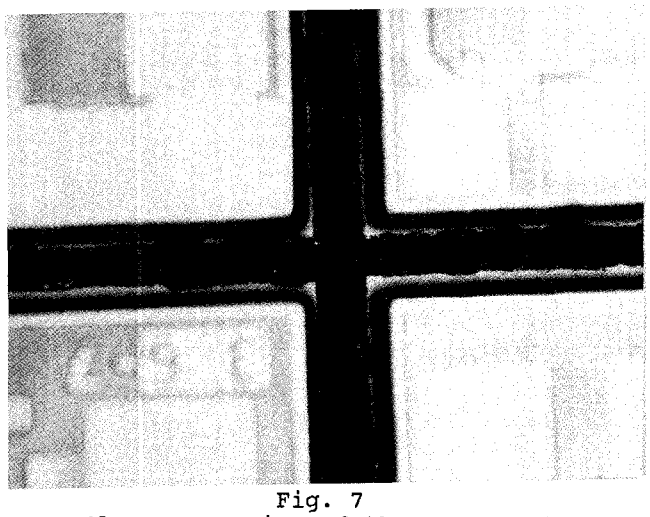

Fig. 7
Close up view of the Laser cut before the wafer is expanded.

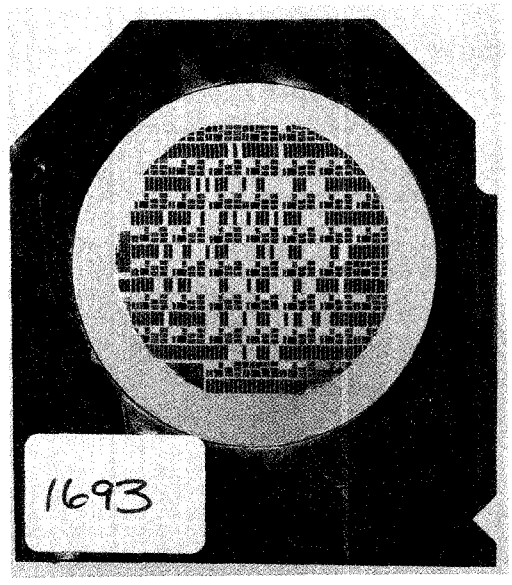

Fig. 8
Laser scribed wafer stretched for sort and load operation.

CONCLUSION

A very repeatable and high yield (100%) laser chip separation process has been developed for the prototype MMIC wafers. This process significantly improves the productivity of the prototype Development Phase. Some of the advantages of this technique can be summarized as follows: (1) Eliminating the chip layout constraint; (2) Reducing the number of wafers required to meet chip demands by 2 to 3 times; (3) Eliminating physical damages to the chip since no pressure or mechanical force is applied to the wafer for chip separation; (4) Minimizing chip handling problems since automatic sort-and-load machine can be used; and (5) Compatible to wafers with and without backside via holes.

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REFERENCE

(1) S.J. Oberg "Laser-Drilled Through-Wafer Vias for GaAs Microwave Devices", paper No. 592 SOA, SOTAPOCS VI The Electrochemical Society, Philadelphia, Pennsylvania Meeting, May, 1987.